Molecular Logic

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Electrically Addressable Multistate Volatile Memory with Flip-Flop and Flip-Flap-Flop Logic Circuits on a Solid Support**

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Molecules that can perform complex mathematical operations are a potential alternative for transistor-type semiconductors.[1] Since a molecular AND gate was demonstrated in 1993,[2] logic gates,[3] circuits,[4] and even molecular memory elements have been reported.[5] Most systems feature solution-based chemistry that inherently suffers from amassing chemical entities, thus compromising on operability and reversibility. Nevertheless, molecular information processing is becoming increasingly popular, since molecules are versatile synthetic building blocks for a bottom-up approach for information transfer and storage.[6] In particular, the field of molecular logic has attracted much attention.[1,7] The behavior of molecules as logic gates that respond to specific inputs has found potential applications in sensors,[8] medical diagnostics,[9] molecular memory devices,[5] and molecular computational identification (MCID) tags.[10] To date, the applied logic is almost exclusively based on the underlying principle of mathematical operations performed on a system that can exist exclusively in two stable states, as introduced by George Boole.[11] The ease of fabrication and wide variety of applications of binary systems has made them the status quo for (molecular) information processing technology.

However, in order to cope with an ever-increasing information density, the viability of the binary numeral system also has to be considered. It is well-established that base three is the most efficient numeral system for transferring and storing information[12] (see the Supporting Information). For instance, the information density in a ternary system is approximately 1.6 times higher than in a binary system.[13] Therefore, exploration of molecular-based systems that are capable of existing in multiple states is highly desirable. The exploration of ternary memory devices is of particular interest, since it is expected that they eventually will replace the conventional flip-flop architecture in static random access memory (SRAM).[14]

Multivalue logic or multistate memory has rarely been demonstrated with molecular-based systems.[10,15] Herein we present a reconfigurable binary memory, and the first example of a ternary memory device constructed from a molecular-based assembly on a solid support.[16] Fascinatingly, the assembly mimics both the well-known flip-flop logic circuit, commonly found in SRAM,[17] and the even more interesting ternary flip-flap-flop logic circuit.[18] The latter system enabled the storage of bits (binary digits) and trits (ternary digits) on a reconfigurable molecular-based assembly on a solid support. Furthermore, four- and five-state memory devices could be constructed for applications in dynamic random access memory (DRAM). The electrical addressability ensures chemical reversibility and stability, whereas the optical readout is fast and nondestructive. This result unequivocally demonstrates the proof-of-principle that the electrically addressable assemblies are capable of performing complex mathematical operations, and as such, brings us one step further towards the development of alternatives for transistor-type memory devices.

The molecular memory was constructed from an assembly formed by alternating deposition of **1**[19] and $PdCl_2$ on indium tin oxide (ITO) coated glass functionalized with a pyridyl-group terminated monolayer (Scheme 1). Because the optical output is a precise function of the applied potential, the optical properties can be accurately controlled (Figure S1 in the Supporting Information). Therefore, multivalued information can be written on to the assembly by applying specific potential biases (vs. Ag/AgCl). The read–write cycle is completed by monitoring the metal-to-ligand charge-transfer (MLCT) band at $\lambda = 510$ nm,[19a] which can be read out by a conventional UV/Vis spectrophotometer. Interestingly, the read–write operations are fundamentally different, that is, optical and electrochemical, respectively. The optical readout is nondestructive and allows for instantaneous data transfer.

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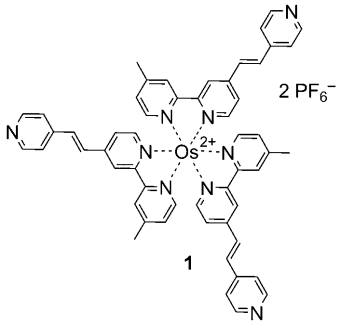


Scheme 1. Molecular structure of **1**.

Binary memory can be constructed by applying double-potential steps between 0.60 and 1.30 V. The assembly is fully reduced and in state 0 when a potential of 0.60 V is applied. However, application of a potential of 1.30 V results in full oxidation of the assembly and, consequently, leads to state 1. Consecutive modulation of these two potentials, with subsequent monitoring of the MLCT band at $\lambda = 510$ nm, leads to read–write cycles of state 1 and 0, respectively (Figure 1a).

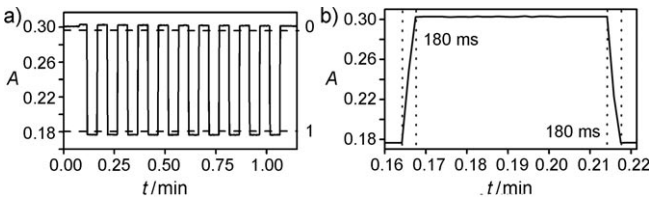


Figure 1. a) Absorbance of the MLCT band at $\lambda = 510$ nm of the **1**-based assembly (17 layers; ca. 31 nm thick) as a function of time upon applying double-potential steps between 0.60 and 1.30 V with 3 s intervals. The dotted lines indicate the two attainable different states. b) Response time ($\Delta A > 95\%$) of the **1**-based assembly (19 layers; ca. 35 nm thick) upon changing from state 0 to state 1 and vice versa.

The system is inherently bistable, however, adventitious amounts of water induce the reduction from Os^{3+} to Os^{2+}.[20] This process is sufficiently slow (25 min for full conversion) so that the assembly can be used for the demonstration of memory functionality. Therefore, no continuously applied potential is needed, since the relatively slow kinetic effect ensures the preservation of the corresponding state within a certain time period with predefined threshold values. A short potential pulse (180 ms) is sufficient to interconvert between the two forms (Figure 1b and Figure S2 in the Supporting Information).

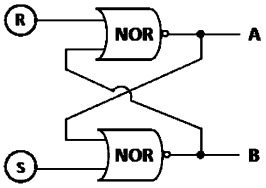
The presence or absence of the two applied input potentials is defined as 1 or 0, respectively. The logic output 1 is defined when the assembly is fully oxidized (Os^{3+}; $A \approx 0.17$), whereas a 0 is produced when the assembly is fully reduced (Os^{2+}; $A \approx 0.30$), provided the absorption remains between the predefined threshold values (see the Supporting Information). In between those two values no stable state exists and the output is undefined. The behavior of the assembly resembles a circuit of two cross-coupled NOR gates that act as a flip-flop device in conventional electronics (Table 1).[18b] Note that even in these systems, the stored data is eventually lost, since we are dealing with volatile memory.

A potential of 1.30 V will fully oxidize the assembly and will set the flip-flop in state 1, whereas a potential of 0.60 V will reset the flip-flop to state 0. When both potentials are absent, the circuit will keep its previous state during a retention time of 150 seconds. The response time of the flip-flop ($> 95\%$ ΔA response) is 180 ms upon application of an electrical potential (Figure 1b). As opposed to our previously reported chemically operated flip-flop circuit,[11a] which is monolayer-based, the inputs used in this study are entirely electrical. As recently highlighted, the state of the art is leading towards solid-state molecular-based logic gates and circuits.[7a] Moreover, the new system has a response time that is 2000 times faster than the chemically addressable system, is subsequently easier to reset, and moreover resembles more conventional transistor-type memories. In addition, the absorption of the multilayer is significantly higher than in a monolayer-based assembly.[5a] This increase results in a good signal-to-noise ratio that allows for the fabrication of multi-state memory (Figure S1 in the Supporting Information).

Table 1: Characteristics table of the **1**-based assembly operating as a set/reset flip-flop.[a]

No.	Inputs		Output	
	R	S	A B	Overall
1	0	0	previous state	
2	0	1	1 0	1
3	1	0	0 1	0

[a] Inputs are 1.30 V (set) and 0.60 V (reset). Note that only one input can be active at a time. Output A corresponds to the absorbance value at $\lambda = 510$ nm.

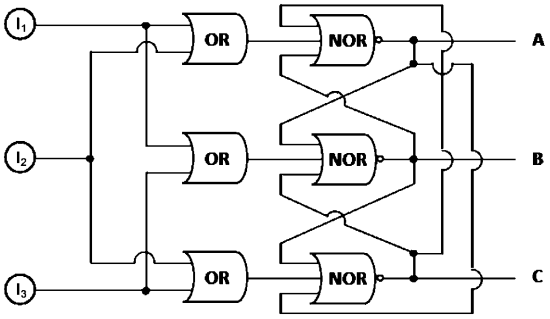


The principles described above can be used to construct a balanced ternary memory with the same **1**-based assembly. Application of a triple-potential step results in three distinct absorption values: a potential of 1.30 V results in full oxidation of the assembly ($A \approx 0.17$), whereas a potential of 0.60 V results in full reduction of the assembly ($A \approx 0.30$). However, when a potential of 0.91 V is applied, the assembly is neither fully oxidized nor fully reduced, and the absorbance is approximately 0.24 (Table 2, Figure 2). The ternary memory can be represented by the sequential logic flip-flap-flop circuit similar to the above-mentioned flip-flop device.

Table 2: Characteristics table of the flip-flap-flop device.[a]

No.	Inputs			Output	
	I_1	I_2	I_3	A B C	Overall
1	0	0	0	previous state	
2	0	0	1	1 0 0	+1
3	0	1	0	0 1 0	0
4	1	0	0	0 0 1	−1

[a] Inputs are 1.30 V (I_1), 0.91 V (I_2), and 0.60 V (I_3). Note that only one input can be active at a time. Outputs −1, 0, and 1 correspond to the different absorption values of the MLCT band at $\lambda = 510$ nm.



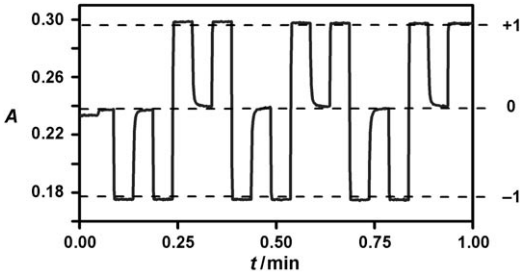


Figure 2. Absorbance of the MLCT band at $\lambda = 510$ nm of the **1**-based assembly (17 layers; ca. 31 nm thick) as a function of time upon applying triple-potential steps at 3 s intervals. The dotted lines indicate the three different states attainable (see Table 2).

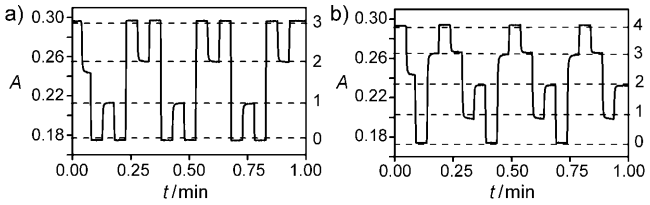


Figure 3. a) Four-state memory generated by applying quadruple-potential steps of 0.60, 0.89, 0.95, and 1.30 V with subsequent monitoring of the MLCT band at $\lambda = 510$ nm of the **1**-based assembly (17 layers; ca. 31 nm thick). b) Five-state memory generated by applying quintuple-potential steps of 0.60, 0.87, 0.92, 0.99, and 1.30 V with subsequent monitoring of the MLCT band at $\lambda = 510$ nm of the assembly (17 layers; ca. 31 nm thick). The dotted lines indicate the four and five different states attainable.

Although the logic circuit is binary, it functions as a ternary memory unit, since it can accept three different inputs, and yields three different outputs that can be stored accordingly.

The circuit is constructed from two connected parts: the first part uses three OR gates that convert the input sequence from I_1, I_2, and I_3 into an appropriate input for the three cross-coupled NOR gates (second part), which provide the memory of the given inputs. For example, when I_1 is applied (1.3 V), the assembly is fully oxidized and the system is in state -1 (output string 0 0 1). In contrast, when I_3 (0.60 V) is applied, the assembly is fully reduced and it is in state $+1$ (output string 1 0 0). However, when input I_2 (0.91 V) is applied, the system is neither fully oxidized nor fully reduced, and remains in state 0 (output string 0 1 0). When none of the inputs are active, the system remains in its previous state, within the boundaries of the threshold values (see the Supporting Information). The retention times of the -1, 0, and 1 states are 75 and 110 seconds, and infinite, respectively. With respect to the access time (180 ms) and within the timeframe over which the potential is applied (3 sec), the retention times are considerable and no immediate refresh is required. It is noteworthy, that in this case the assembly is of mixed valency, that is Os^{2+} and Os^{3+}, respectively. Therefore, the multivalued information is processed by the entire assembly, rather than by the individual molecules, which have only two distinct states.[21] The characteristics table of the logic circuit is shown in Table 2. The analogy to the flip-flop is easily demonstrated, since removal of I_2 results in the sequential logic circuit shown in Figure 1 b.

The observed decrease in retention time upon increasing the number of states currently prohibits the formation of static memory devices that are able to store more than three states. We have explored memory devices with the **1**-based assembly that are able to store four and five states (Figure 3). The retention time of these systems may allow for the fabrication of DRAM, which has typical refresh rates in the millisecond region.[22] In general, the retention times can be enhanced by the exclusion of trace amounts of H_2O that is responsible for the reduction of the Os^{3+} metal centers.[21] Integration of the **1**-based assembly into a solid-state device will further improve the retention times, and might allow for the fabrication of memory devices that can store multivalued digits.

In conclusion, we have shown that electrochromic materials,[19a,23] and in particular the **1**-based assembly, are suitable platforms for the construction of multivalued SRAM devices. These systems can be cycled at least 1000 times without any significant data loss,[19a] which is orders of magnitude larger than chemically addressable systems.[5a] Accurate control of the optical properties by an applied electric field enabled us to divide the absorbance of the **1**-based assembly into distinct regions, which serve as the memory states of the device. In addition, these memory functions can be represented by highly complex sequential logic circuits. In particular, flip-flop and flip-flap-flop circuits have been mimicked upon reconfiguration of the input potentials. This research demonstrates the potential use of electrochromic materials in multivalued memory devices and logic gates. We believe that the principles demonstrated here are applicable to electrochromic materials that are commonly available. The differentiation of multiple states requires the strict definition of threshold values. Therefore, future research will be directed towards integrating thicker assemblies into solid-state setups with higher ON/OFF ratios that might allow for increased storage capacity, better signal-to-noise ratios, and/or higher retention times.

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